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=> d his

     (FILE 'USPAT' ENTERED AT 16:44:36 ON 28 JUN 1999)
L1         32550 S SUBSTRATE# (P) (DIELECTRIC OR PLASMA ETCH?)
L2          5566 S L1 (P) CONDUCTOR#
L3             9 S L2 (P) HARD MASK#
L4             9 S L3 AND PHOTORESIST#
L5           349 S 216/2/CCLS
L6             0 S L4 AND L5
L7           922 S 216/67/CCLS
L8             0 S L4 AND L7
L9            28 S 216/74/CCLS
L10          181 S 216/75/CCLS
L11          101 S 216/76/CCLS
L12            0 S L4 AND L9
L13            0 S L4 AND L10
L14            0 S L4 AND L11
L15            5 S L9 AND L10
L16            1 S L15 AND L11
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=> s 216/clas

L17 9232 216/CLAS

=> s l17 and l4

L18 2 L17 AND L4

=> d l18 1-

1. 5,173,442, Dec. 22, 1992, Methods of forming channels and vias in insulating layers; David H. Carey, **216/18**, **41**; 430/312; 438/620, 633, 702, 940 [IMAGE AVAILABLE]

2. 5,091,339, Feb. 25, 1992, Trenching techniques for forming vias and channels in multilayer electrical interconnects; David H. Carey, **216/18**, **48**; 430/312; 438/623, 631, 940, 945 [IMAGE AVAILABLE]

=> d 14 1-

1. 5,899,736, May 4, 1999, Techniques for forming electrically blowable fuses on an integrated circuit; Peter Weigand, et al., 438/601, 467 [IMAGE AVAILABLE]

2. 5,670,018, Sep. 23, 1997, Isotropic silicon etch process that is highly selective to tungsten; Elke Eckstein, et al., 438/714, 715, 719, 723, 963 [IMAGE AVAILABLE]

3. 5,661,344, Aug. 26, 1997, Porous dielectric material with a passivation layer for electronics applications; Robert H. Havemann, et al., 257/758, 637, 642, 759, 760 [IMAGE AVAILABLE]

4. 5,654,240, Aug. 5, 1997, Integrated circuit fabrication having contact opening; Kuo-Hua Lee, et al., 438/647, 586, 669 [IMAGE AVAILABLE]

5. 5,472,913, Dec. 5, 1995, Method of fabricating porous dielectric material with a passivation layer for electronics applications; Robert H. Havemann, et al., 438/702, 624, 631, 763 [IMAGE AVAILABLE]

6. 5,173,442, Dec. 22, 1992, Methods of forming channels and vias in insulating layers; David H. Carey, 216/18, 41; 430/312; 438/620, 633, 702, 940 [IMAGE AVAILABLE]

7. 5,091,339, Feb. 25, 1992, Trenching techniques for forming vias and channels in multilayer electrical interconnects; David H. Carey, 216/18, 48; 430/312; 438/623, 631, 940, 945 [IMAGE AVAILABLE]

8. 5,057,443, Oct. 15, 1991, Method for fabricating a trench bipolar transistor; Louis N. Hutter, 438/330, 331, 360 [IMAGE AVAILABLE]

9. 4,929,996, May 29, 1990, Trench bipolar transistor; Louis N. Hutter, 257/552, 514 [IMAGE AVAILABLE]

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US PAT NO: 5,899,736 [IMAGE AVAILABLE] L4: 1 of 9
TITLE: Techniques for forming electrically blowable fuses on an integrated circuit

SUMMARY:

BSUM(10)

Above silicon nitride layer 108, a **photoresist** layer 110 is deposited and patterned to form an opening 112. Patterned **photoresist** mask 110 is then employed to etch through silicon nitride layer 108 to expose a portion of oxide layer 106. . .

SUMMARY:

BSUM(13)

It . . . decreases in width and the adjacent fuses and/or devices are packed closer together, the accurate alignment of opening 112 in

photoresist layer 110 with fuse portion 102 becomes increasingly difficult. These and other challenges presented by the photolithography step render the. . .

DETDESC:

DETD(12)

FIG. . . . of the present invention, the steps employed in the formation of a typical electrically blowable fuse. In step 702, a **substrate** is provided. As mentioned, the **substrate** may represent a silicon **substrate** on which devices have already been formed. In step 704, a fuse portion, e.g., a **conductor** formed of a fuse material, is formed. In steps 706 and 708, the first and second **dielectric** layers are conformally deposited. In step 710, a CMP step is employed to polish through the second **dielectric** layer at the protruded spot to expose a portion of the underlying first **dielectric** layer. In step 712, a microcavity etch step is employed to etch a microcavity in the first **dielectric** layer through the opening in the **hard mask**/second **dielectric** layer while leaving the **hard mask** and the fuse portion substantially unetched. In step 714, a third **dielectric** layer representing a plug layer is deposited to close up the opening in the **hard mask**/second **dielectric** layer, thereby sealing the microcavity from the outside.

US PAT NO: 5,670,018 [IMAGE AVAILABLE] L4: 2 of 9
TITLE: Isotropic silicon etch process that is highly selective to tungsten

SUMMARY:

BSUM(10)

Anisotropic processes using HBr as a single species etchant for etching silicon and polysilicon selective to a **photoresist** have also been utilized, however, these processes are not very selective to tungsten. Also, because they are also anisotropic, they. . .

DETDESC:

DETD(4)

The structure of FIG. 1 will now be described. The semiconductor device 10 comprises a **substrate** 14 on which gate **conductors** 11 have been formed. The gate **conductors** 11 are covered by a gate-cap **dielectric** 16 of silicon nitride or silicon dioxide, and over this structure is formed a mandrel polysilicon layer 13 which is planarized by chemical-mechanical polishing (CMP) to the level of the gate-cap **dielectric**. This mandrel polysilicon layer is then extended as a polysilicon layer 15. A **hard-mask** oxide layer 18 is formed over the extended layer 15 to define openings to be formed in the polysilicon layers. . .

US PAT NO: 5,661,344 [IMAGE AVAILABLE] L4: 3 of 9
TITLE: Porous dielectric material with a passivation layer for electronics applications

DETDESC:

DETD(3)

As . . . invention). Conducting layer 12 may be connected through insulating layer 10 to an underlying structure (not shown). A layer of **photoresist** 14 is spun on over conducting layer 12, exposed through a mask pattern and developed, such that the **photoresist** layer 14

contains gaps 16 where conducting layer 11 is to be removed. Referring now to FIG. 1B, conducting material has been removed using an etching process which removes material below gaps in the **photoresist** layer to create patterned conductors 18 separated by gaps 20. The **photoresist** 14 of FIG. 1A has also been stripped and does not appear in FIG. 1B. FIG. 1C shows additional layers. . .

DETDESC:

DETD(6)

A . . . for both cap layer 24 and underlying porous layer 22 may be examined. FIG. 1C shows a new layer of **photoresist** 26 deposited over cap layer 24. A via 28 is shown after mask patterning and developing of **photoresist** layer 26, and after anisotropic etch of cap layer 24.

DETDESC:

DETD(8)

FIG. 1D illustrates the device after **photoresist** 26 has been stripped and via 28 has been etched through dielectric layer 22 to conductor 18. Such an etch. . .

DETDESC:

DETD(13)

Drawing Element	Preferred or Specific Examples	Generic Term	Other Alternate Examples
10	SiO.sub.2	**Substrate**	Other oxides, P-glass, silicon nitride
18,38	AlCu alloy with TiN underlayer and overlayer	Patterned **conductors**	Al, Cu, Mo, W, Ti, alloys of these, polysilicon, silicides, nitrides, carbides
14,26		**Photoresist**	
22,40	Surface-modified dried gel	Porous **dielectric** layer	Supercritically-dried aerogel, other fine-pored porous dielectrics
24,42	Silicon dioxide	Cap layer. . .	
30	Silicon dioxide	Via passivation layer	Other oxides, silicon nitride, silicon oxynitride
32,36	Silicon dioxide	**Substrate** encapsulation layer	Other oxides, silicon nitride, silicon oxynitride
34	Silicon nitride	**Hard mask** layer	

US PAT NO: 5,654,240 [IMAGE AVAILABLE] L4: 4 of 9
TITLE: Integrated circuit fabrication having contact opening

ABSTRACT:
A method of semiconductor fabrication having applicability to forming contacts to sources and drains especially in SRAM applications is disclosed. A **dielectric** and an overlying polysilicon **conductor** are formed and patterned thereby exposing a semiconductor **substrate**. A silicide layer is deposited, thereby contacting the polysilicon layer and the **substrate**. Subsequent patterning of the silicide layer using an oxide **hard mask** provides electrical contact between the polysilicon layer and the **substrate** without the risk of trenching into the **substrate**.

SUMMARY:

BSUM(7)

FIGS. . . . to cover exposed surface 29 of junction 25. It is desired that polysilicon layer 31 should be patterned using a **photoresist**. **Photoresist** 33 is subsequently deposited over polysilicon layer 31 and patterned. It is desirable that edge 35 of **photoresist** 33 be immediately above (or, in FIG. 4, to the left of) edge 37 of patterned dielectric 27.

SUMMARY:

BSUM(8)

Should edge 35 of **photoresist** 33 be slightly misaligned (and, as shown in FIG. 4, somewhat to the right of edge 37 of dielectric 27,. . . layer 27), subsequent etching will stop on dielectric 27 and not damage junction 25. However, should patterned edge 35 or **photoresist** 33 be to the right of patterned edge 37 of dielectric 27, the trench 39 depicted in FIG. 5 may. . .

DETDESC:

DETD(5)

It . . . with (or to the left of) the edges of dielectrics 131 and 127. That is, turning to FIG. 9, after **photoresist** 135 is deposited and spun, **photoresist** 135 is patterned creating edge 136. Ideally, edge 136 is co-linear with edge 137 of layers 131 and 127, respectively.. . .

DETDESC:

DETD(6)

Returning to FIG. 9, unfortunately, it is not always possible, because of alignment tolerances, to pattern **photoresist** 135 so that edge 136 is precisely co-linear with edge 137 of layers 131 and 127. Sometimes, edge 136 will. . .

DETDESC:

DETD(7)

FIGS. 11 and 12 illustrate what happens when edge 136 of **photoresist** 135 is positioned, because of misalignment tolerances, to the left of edge 137. In other words, patterned edge 136 of **photoresist** 135 does

not overlie the opening created by edge 137 over substrate 123.

DETDESC:

DETD(9)

It . . . noted that, in the situations depicted in FIGS. 9-10 and 11-12 (i.e., those situations in which the edge of the **photoresist** mask is outside or coincident with the edge of the opening defined by layers 127 and 131), that no problem. . . occur, even if more conventional processing techniques described in FIGS. 2-5 are employed. However, should the defining edge 136 of **photoresist** 134 overlie the openings defined by edge 137 of layers 127 and 131, use of the technique described in FIGS.. . .

DETDESC:

DETD(10)

In FIG. 13, it will be noted that edge 136 of **photoresist** 135 is slightly interior to edges 137. That is, edge 136 overlies the opening over substrate 123 defined by edge. . .

DETDESC:

DETD(14)

In . . . silicide layer 132 is etched during the removal of polysilicon layer 131. Should (returning to FIG. 16) edge 136 of **photoresist** 135 be positioned too far to the right, i.e., too far to the interior of the opening defined by edge. . .

US PAT NO: 5,472,913 [IMAGE AVAILABLE] L4: 5 of 9
TITLE: Method of fabricating porous dielectric material with a passivation layer for electronics applications

DETDESC:

DETD(3)

As . . . invention). Conducting layer 12 may be connected through insulating layer 10 to an underlying structure (not shown). A layer of **photoresist** 14 is spun on over conducting layer 12, exposed through a mask pattern and developed, such that the **photoresist** layer 14 contains gaps 16 where conducting layer 12 is to be removed. Referring now to FIG. 1B, conducting material has been removed using an etching process which removes material below gaps in the **photoresist** layer to create patterned conductors 18 separated by gaps 20. The **photoresist** 14 of FIG. 1A has also been stripped and does not appear in FIG. 1B. FIG. 1C shows additional layers. . .

DETDESC:

DETD(6)

A . . . for both cap layer 24 and underlying porous layer 22 may be examined. FIG. 1C shows a new layer of **photoresist** 26 deposited over cap layer 24. A via 28 is shown after mask patterning and developing of **photoresist** layer 26, and after anisotropic etch of cap layer 24.

DETDESC:

DETD(8)

FIG. 1D illustrates the device after **photoresist** 26 has been

stripped and via 28 has been etched through dielectric layer 22 to conductor 18. Such an etch. . .

DETDESC:

DETD(13)

Drawing Element	Preferred or Specific Examples	Generic Term	Other Alternate Examples
10	SiO.sub.2	**Substrate**	Other oxides, P-glass, silicon nitride
18,38	AlCu alloy with TiN underlayer and overlayer	Patterned **conductors**	Al, Cu, Mo, W, Ti, alloys of these, polysilicon, silicides, nitrides, carbides
14,26		**Photoresist**	
22,40	Surface-modified dried gel	Porous **dielectric** layer	Supercritically-dried aerogel, other fine-pored porous dielectrics
24,42	Silicon dioxide Cap. . . Via passivation layer	Silicon dioxide	Other oxides, silicon nitride, silicon oxynitride
32,36	Silicon dioxide encapsulation layer	**Substrate**	Other oxides, silicon nitride, silicon oxynitride
34	Silicon nitride	**Hard mask** layer	Silicon oxynitride

US PAT NO: 5,173,442 [IMAGE AVAILABLE] L4: 6 of 9
TITLE: Methods of forming channels and vias in insulating layers

ABSTRACT:
Channels extending partially through and vias extending completely through an insulating layer in an electrical interconnect such as a **substrate** or integrated circuit can be formed in a relatively few steps with low cost etching and patterning techniques. The channels and vias can then be filled with an electrical **conductor** in a relatively few steps. In one embodiment a non-erodible **hard mask** exposing the vias and channels is placed over a polyimide layer, an erodible soft mask exposing the vias but covering the channels is placed over the

hard mask, and a **plasma etch** is applied. The via regions are etched until the soft mask completely erodes and then both the via and channel. . . the seed layer substantially filling the channels and vias. The interconnect surface is then planarized by polishing until the electrical **conductor** remains only in the channels and vias.

DETDESC:

DETD(5)

FIGS. 1a-1f show a first embodiment for forming the **conductor** channels and vias. In FIG. 1a a thin blanket layer of metal such as 2500 angstroms copper over 700 angstroms chromium is sputtered over polyimide layer 14 to form **hard mask** 16, which after conventional patterning has openings to expose via regions 20 and channel regions 22. In FIG. 1b soft mask 18 of **photoresist**, which can also be silicon-dioxide or silicon-nitride, is placed over **hard mask** 16 and after conventional patterning has openings to expose via regions 20 but covers channel regions 22. Thus via regions 20 are exposed but channel regions 22 are not exposed. In FIG. 1c a suitable etch is applied wherein **hard mask** 16 is non-erodible but soft mask 18 erodes. For illustration purposes a dry etcher can generate **plasma etch** 24. That is, as **plasma etch** 24 is applied **hard mask** 16 etchs slowly or not at all while soft mask 18 etchs rapidly and merely causes a time delay until. . . are intended to be 10 microns deeper than channel regions 22, so soft mask 18 can be 10 microns thick **photoresist** provided it etches at the same rate as underlying polyimide layer 14. Thus the thickness of soft mask 18 can be adjusted for differential etch rates between soft mask 18 and underlying polyimide 14. **Plasma etch** 24 can comprise 90% O.sub.2 and 10% SF6 at 600 watts RF power and 150 millitorrs pressure, although the parameters for **plasma etch** 24 such as power, pressure, chemistry, and electrode spacing are highly variable depending on the desired etch rates, profiles, and. . . via regions 20 begin to etch channel regions 22 remain covered and undisturbed, and soft mask 18 begins to erode. **Plasma etch** 24 will tend to etch vertically and attack the exposed surfaces at the same rate. FIG. 1d shows soft mask. . . 20 partially etched through polyimide layer 14. If desired, via regions 20 could be fully etched at this stage. As **plasma etch** 24 continues, FIG. 1e shows via regions 20 etched 15 microns through the entire thickness of polyimide layer 14, and. . . and improved step coverage vias from less vertical sidewall slopes. Sloped via sidewalls may be difficult to accomplish with a **hard mask** and a dry etch since the plasma may etch anisotropically. In FIG. 1f **plasma etch** 24 is discontinued and **hard mask** 16 is removed from polyimide layer 14. Via regions 20 and channel regions 22 are now formed. **Substrate** 10 may now require surface cleaning if contamination develops from etch products not carried away by the etch process. The. . .

DETDESC:

DETD(8)

FIGS. 2a-2f show a second embodiment for forming the **conductor** channels and vias in which any description for the first embodiment in FIGS. 1a-1f is incorporated herein insofar as the. . . mask 30. Via openings 32 and 36 are aligned to assure proper placement of via regions 20. FIG. 2c shows **plasma etch** 24 applied to upper soft mask 34. As **plasma etch** 24 is applied via regions 20 begin to etch and upper soft mask 34 begins to erode. FIG. 2d shows. . . eroded, lower soft mask 30 eroded over channel regions 22, and via regions 20 partially etched through polyimide layer 14. **Plasma etch** 24 continues, and in FIG. 2e via regions 20 are etched entirely through polyimide layer 14, channel regions 22 are. . . partially eroded, in which case the non-eroded portions remaining after via regions 20 and channel regions 22

are formed and **plasma etch** 24 is discontinued would be removed from **substrate** 10 such as by stripping. The use of two soft masks instead of the soft mask and **hard mask** combination described in the first embodiment is a trade-off since two soft masks require fewer process steps but may require. . .

DETDESC:

DETD(13)

FIGS. . . . In FIG. 4g second plasma etch 24b is discontinued and via regions 20 and channel regions 22 are formed. If **photoresist** from mask 37 or 38 remains then it is stripped.

US PAT NO: 5,091,339 [IMAGE AVAILABLE] L4: 7 of 9
TITLE: Trenching techniques for forming vias and channels in multilayer electrical interconnects

ABSTRACT:
Channels extending partially through and vias extending completely through an insulating layer in an electrical interconnect such as a **substrate** or integrated circuit can be formed in a relatively few steps with low cost etching and patterning techniques. The channels and vias can then be filled with an electrical **conductor** in a relatively few steps. In one embodiment a non-erodible **hard mask** exposing the vias and channels is placed over a polyimide layer, an erodible soft mask exposing the vias but covering the channels is placed over the **hard mask**, and a **plasma etch** is applied. The via regions are etched until the soft mask completely erodes and then both the via and channel. . . the seed layer substantially filling the channels and vias. The interconnect surface is then planarized by polishing until the electrical **conductor** remains only in the channels and vias.

DETDESC:

DETD(5)

FIGS. 1a-1f show a first embodiment for forming the **conductor** channels and vias. In FIG. 1a a thin blanket layer of metal such as 2500 angstroms copper over 700 angstroms chromium is sputtered over polyimide layer 14 toform **hard mask** 16, which after conventional patterning has openings to expose via regions 20 and channel regions 22. In FIG. 1b soft mask 18 of **photoresist**, which can also be silicon-dioxide or silicon-nitride, is placed over **hard mask** 16 and after conventional patterning has openings toexpose via regions 20 but covers channel regions 22. Thus via regions 20 are exposed but channel regions 22 are not exposed. In FIG. 1c a suitable etch is applied wherein **hard mask** 16 is non-erodible but soft mask 18 erodes. For illustration purposes a dry etcher can generate **plasma etch** 24. That is, as **plasma etch** 24 is applied **hard mask** 16 etchs slowly or notat all while soft mask 18 etchs rapidly and merely causes a time delay until plasma. . . are intended to be 10 microns deeper than channel regions 22, so soft mask 18 can be 10 microns thick **photoresist** provided it etches at the same rate as underlying polyimide layer 14. Thus the thickness of soft mask 18 can be adjusted fordifferential etch rates between soft mask 18 and underlying polyimide 14. **Plasma etch** 24 can comprise 90% O.sub.2 and 10% SF.sub.6 at 600 watts RF power and 150 millitorrs pressure, although the parameters for **plasma etch24** such as power, pressure, chemistry, and electrode spacing are highly variable depending on the desired etch rates, profiles, and etcher. . . via regions 20 begin to etch channel regions 22 remain covered and undisturbed, and soft mask 18 begins to erode. **Plasma etch** 24 will tend to etch vertically and attack the exposed surfaces at the same rate. FIG. 1d shows soft mask. . . 20 partially etched through polyimide layer 14. If desired, via regions 20

could be fully etched at this stage. As **plasma etch** 24 continues, FIG. 1e shows via regions 20 etched 15 microns through the entire thickness of polyimide layer 14, and. . . slopes and improved step coverage vias from less vertical sidewall slopes.Sloped via sidewalls may be difficult to accomplish with a **hard mask** and a dry etch since the plasma may etch anisotropically. In FIG. 1f **plasma etch24** is discontinued and **hard mask** 16 is removed from polyimide layer 14. Viaregions 20 and channel regions 22 are now formed. **Substrate** 10 may now require surface cleaning if contamination develops from etch products not carried away by the etch process. The. . .

DETDESC:

DETD(8)

FIGS. 2a-2f show a second embodiment for forming the **conductor** channels andvias in which any description for the first embodiment in FIGS. 1a-1f is incorporated herein insofar as the same. . . mask 30. Via openings 32 and 36 are aligned to assure proper placement of via regions 20. FIG. 2c shows **plasma etch** 24 applied to upper soft mask 34. As **plasma etch** 24 is applied via regions 20 begin to etch and upper soft mask 34 begins to erode. FIG. 2d shows. . . completely eroded, lower soft mask 30 eroded over channel regions 22, and via regions20 partially etched through polyimide layer 14. **Plasma etch** 24 continues, and in FIG. 2e via regions 20 are etched entirely through polyimide layer 14, channel regions 22 are. . . partially eroded, in which case the non-eroded portions remaining after via regions 20 and channel regions 22 are formed and **plasma etch** 24 is discontinued would be removed from **substrate** 10 such as by stripping. The use of two soft masks instead of the soft mask and **hard mask** combination described in the first embodiment is a trade-off since two soft masks require fewer process steps but may require. . .

DETDESC:

DETD(13)

FIGS. . . . In FIG. 4g second plasma etch 24b is discontinued and via regions 20 and channel regions 22 are formed. If **photoresist** from mask37 or 38 remains then it is stripped.

CLAIMS:

CLMS(5)

5. The method of claim 1 wherein the soft mask is a material selected from the group consisting of **photoresist**, silicon-dioxide, and silicon-nitride.

CLAIMS:

CLMS(10)

10. . . . insulating layer is polyimide and the upper and lower soft masks are a material selected from the group consisting of **photoresist**, silicon-dioxide, and silicon-nitride, and further comprising the step of:
removing any portions of the first or second soft masks that. . .

CLAIMS:

CLMS(14)

14. . . . insulating layer is polyimide and the first and second soft masks are a material selected from the group consisting of

photoresist, silicon-dioxide, and silicon-nitride, and further comprising the step of:
removing any portions of the first or second soft masks that. . .

CLAIMS:

CLMS(18)

18. . . . insulating layer is polyimide and the first and second soft masks are a material selected from the group consisting of **photoresist**, silicon-dioxide, and silicon-nitride, and further comprising the step of:
removing any portions of the first or second soft masks that. . .

CLAIMS:

CLMS(44)

44. . . . insulating layer is polyimide and the first and second soft masks are a material selected from the group consisting of **photoresist**, silicon-dioxide, and silicon-nitride, and further comprising the step of:
removing any portions of the first or second soft masks that. . .

US PAT NO: 5,057,443 [IMAGE AVAILABLE] L4: 8 of 9
TITLE: Method for fabricating a trench bipolar transistor

DETDESC:

DETD(5)

A **photoresist** layer 16 is next spun or otherwise deposited over the surface of the wafer and patterned to define one or more openings 18 to locate trench depressions within the substrate 10. More particularly, the **photoresist** 16 is patterned to define areas for the removal of the exposed hard mask layer portions 14. An oxide dry. . . the plasma type, is then conducted to effect a removal of the hard mask within the areas patterned by the **photoresist** 16.

DETDESC:

DETD(6)

FIG. 2 illustrates the wafer after the patterning of the hard mask layer 14. The **photoresist** 16 is removed and the hard mask layer 14 then functions as a mask for the subsequent etching of the. . .

DETDESC:

DETD(18)

As . . . process, in which P-type impurities are diffused into the exposed areas of the epitaxial material 40, as well as the **substrate** 10. In the alternative, an ion implant process can be utilized to construct the P-type semiconductor regions. Formed within the. . . base region of the NPN transistor of the invention. Significantly, the base region 44 is formed self-aligned according to the **hard mask** 14. According to another important feature of the invention, the base region 44 is separated from the vertical collector **conductor** 32 by only the thickness of the sidewall **dielectric** 34. A more compact transistor can thus be realized.

CLAIMS:

CLMS(24)

24. . . . 19, further including forming channel stop areas of said first and second implants with different type impurities and without a **photoresist** masking step.

US PAT NO: 4,929,996 [IMAGE AVAILABLE] L4: 9 of 9
TITLE: Trench bipolar transistor

DETDESC:

DETD(5)

A **photoresist** layer 16 is next spun or otherwise deposited over the surface of the wafer and patterned to define one or more openings 18 to locate trench depressions within the substrate 10. More particularly, the **photoresist** 16 is patterned to define areas for the removal of the exposed hard mask layer portions 14. An oxide dry. . . the plasma type, is then conducted to effect a removal of the hard mask within the areas patterned by the **photoresist** 16.

DETDESC:

DETD(6)

FIG. 2 illustrates the wafer after the patterning of the hard mask layer 14. The **photoresist** 16 is removed and the hard mask layer 14 then functions as a mask for the subsequent etching of the. . .

DETDESC:

DETD(18)

As . . . process, in which P-type impurities are diffused into the exposed areas of the epitaxial material 40, as well as the **substrate** 10. In the alternative, an ion implant process can be utilized to construct the P-type semiconductor regions. Formed within the. . . base region of the NPN transistor of the invention. Significantly, the base region 44 is formed self-aligned according to the **hard mask** 14. According to another important feature of the invention, the base region 44 is separated from the vertical collector **conductor** 32 by only the thickness of the sidewall **dielectric** 34. A more compact transistor can thus be realized.